WHAT IS CLAIMED IS:

1. A data storage system comprising:

a first memory array including a first plurality of memory cells;

a first decoder circuit for selecting ones of said first plurality of memory cells;

a first sensing circuit to detect using a first sensing mode content of said selected ones of said first plurality of memory cells;

a second memory array including a second plurality of memory cells;

a second decoder circuit for selecting ones of said second plurality of memory cells; and

a second sensing circuit to detect using a second sensing mode content of said selected ones of said second plurality of memory cells.

2. The data storage system of claim 1 wherein the first and second plurality of memory cells are arranged in segments.

3. The data storage system of claim 2 wherein the segments of said first plurality of memory cells are a first size and the segments of said second plurality of memory cells are a second size.

4. The data storage system of claim 1 wherein the first plurality of memory cells store said content therein as multilevel content, and said second plurality of memory cells store said content therein as single level content.

5. The data storage system of claim 1 wherein the first plurality of memory cells store said content therein as multilevel content, and said second plurality of memory cells store said content therein as multilevel content.

6. The data storage system of claim 1, wherein said first memory array stores data and said second memory array stores code.

7. The data storage system of claim 6 wherein said first sensing mode is a voltage sensing mode, and said second sensing mode is a current sensing mode.

8. The data storage system of claim 6 where said first sensing mode is a current sensing mode, and said second sensing mode is a voltage sensing mode.

9. The data storage system of claim 1 further comprising:

a third memory array including a third plurality of memory cells;

a third decoder circuit for selecting a portion of said third plurality of memory cells; and

a third sensing circuit to detect using one of said first and second sensing modes, content of said selected portion of said third plurality of memory cells,

wherein said second plurality of memory cells store said content therein using multilevel storage, and the third plurality of memory cells stores said content therein using single level storage.

10. The data storage system of claim 9 wherein the first plurality of memory cells store data, and said second and third plurality of memory cells store code.

11. The data storage system of claim 9 wherein the first plurality of memory cells store said content therein as multilevel content.

12. The data storage system of claim 9 wherein the first plurality of memory cells store said content therein as single level content.

13. The data storage system of claim 9 further comprising a tag bit array including a plurality of tag bit cells.

14. The data storage system of claim 13 wherein each tag bit cell storing an indication of the content of an associated group of said first, second, and third plurality of memory cells.

15. The data storage system of claim 13 further comprising:

a fourth sensing circuit to detect a tag bit corresponding to said selected ones of said first, second, or third plurality of memory cells to control said first and second sensing modes.

16. A storage system comprising:

a plurality of memory cells; and

a plurality of tag bit cells.

17. The data storage system of claim 16 wherein the memory cells are single level or multilevel.

18. The data storage system of claim 17 wherein the memory cells are nonvolatile.

19. The data storage system of claim 17 wherein the memory cells are volatile.

20. The data storage system of claim 16 wherein the tag bits are single level or multilevel.

21. The data storage system of claim 20 wherein the tag bit cells are nonvolatile or volatile.

22. A data storage system comprising:

a first memory array including a first plurality of memory cells;

a first decoder circuit for selecting ones of said first plurality of memory cells;

a second memory array including a second plurality of memory cells;

a second decoder circuit for selecting ones of said second plurality of memory cells; and

a sensing circuit to selectively detect using a first sensing mode content of said selected ones of said first plurality of memory cells and using a second sensing mode content of said selected ones of said second plurality of memory cells.

23. The data storage system of claim 22 wherein the first and second plurality of memory cells are arranged in segments.

24. The data storage system of claim 23 wherein the segments of said first plurality of memory cells are a first size and the segments of said second plurality of memory cells are a second size.

25. The data storage system of claim 22 wherein the sensing circuit is configurable.

26. The data storage system of claim 25 wherein the sensing circuit is configurable to switch between the first and second sensing modes.

27. The data storage system of claim 25 wherein the sensing circuit is configurable to switch between a high speed and a low speed sensing mode.

28. The data storage system of claim 25 wherein the sensing circuit is configurable to switch between a multilevel sensing mode and a single level sensing mode.

29. The data storage system of claim 22 wherein the first plurality of memory cells store multilevel content, the number of bits stored per cell being configurable, the sensing circuit being configurable to the adjustable number of bits of content stored in said first plurality of memory cells.

30. The data storage system of claim 22 wherein the sensing circuit comprises:

a sensing mode configuration circuit coupled to selected ones of the first and second plurality of memory cells to detect content stored in said selected memory cells in said first or second sensing modes;

a first transistor of the first type including first and second terminals with a channel therebetween, and a gate for controlling current in said channel and coupled to the sensing mode configuration circuit, said first terminal being coupled to a supply voltage;

a current source including a first terminal coupled to the second terminal of the first transistor of the first type and a second terminal coupled to ground, a current source providing a bias current; and

a comparator for comparing the voltage on said second terminal of the first transistor of the first type and a reference voltage, and including an output indicative of said comparison.

31. The data storage system of claim 30 wherein the sensing mode configuration circuit comprises:

a first transistor of a second type including first and second terminals with a channel therebetween, and a gate for controlling current in said channel, the second terminal being coupled to one of the selected ones of the first or second plurality of memory cells and coupled to the gate of the first transistor of the first type;

a first switch including a first terminal coupled to a supply voltage and including a second terminal coupled to the first terminal of the first transistor of the second type to selectively couple the supply voltage to said first transistor of the second type in said first sensing mode;

a second switch including a first terminal coupled to the first terminal of the first transistor of the second type, and including a second terminal coupled to the gate of the first transistor of the second type to selectively couple said first terminal of the first transistor of the second type to said gate in said first sensing mode;

a third switch including a first terminal coupled to said selected one of the memory cells and including a second terminal coupled to a ground terminal, to selectively ground said selected memory cell in said first sensing mode;

a fourth switch including a first terminal coupled to the first terminal of the first transistor of the second type and including a second terminal coupled to said ground terminal to selectively couple said first terminal to said ground terminal in said second sensing mode;

a fifth switch including a first terminal coupled to the gate of said first transistor of the second type and including a second terminal coupled to a bias voltage terminal to selectively couple said bias voltage terminal to said gate in said second sensing mode; and

a sixth switch including a first terminal coupled to the supply voltage, including a second terminal coupled to the selected memory cell to selectively couple said memory cell to said supply voltage in said second sensing mode.

32. The data storage system of claim 22 further comprising:

a third memory array including a third plurality of memory cells;

a third decoder circuit for selecting ones of said third plurality of memory cells,

wherein the sensing circuit further selectively detects using said second sensing mode content of said selected ones of said third plurality of memory cells,

wherein said second plurality of memory cells store said content therein using multilevel storage and the third plurality of memory cells stores said content therein using single level storage.

33. The data storage system of claim 32 wherein the sensing circuit is configurable.

34. The data storage system of claim 33 wherein the sensing circuit is configurable to switch between the first and second sensing modes.

35. The data storage system of claim 32 wherein the first, second, third plurality of memory cells are arranged in segments.

36. The data storage system of claim 35 wherein the segments of said first plurality of memory cells are a first size, the segments of said second plurality of memory cells are a second size, and the segments of said third plurality of memory cells are a third size.

37. A data storage system comprising:

a first memory array including a first plurality of memory cells;

a first decoder circuit for selecting a portion of said first plurality of memory cells;

a tag bit memory for storing tag bit indicators of content stored in corresponding cells of the first plurality of memory cells;

a tag bit sensing circuit to detect a selected tag bit indicator corresponding to selected ones of said first plurality of memory cells;

a first sensing circuit to selectively detect using a first or second sensing mode content of said selected portion of said first plurality of memory cells, the first and second sensing mode being determined by the selected tag bit corresponding to the selected memory cells;

a content addressable memory including a second plurality of memory cells;

a second decoder circuit for selecting a portion of said second plurality of memory cells of said content addressable memory; and

a second sensing circuit to detect content of said selected portion of said second plurality of memory cells.

38. The data storage system of claim 37 wherein the first plurality of memory cells are arranged in segments.

39. The data storage system of claim 38 wherein the segments of a first portion of said first plurality of memory cells are a first size and the segments of a second portion of said first plurality of memory cells are a second size.

40. The data storage system of claim 37 wherein the first sensing circuit is configurable.

41. The data storage system of claim 37 further comprising:

an extension array comprising a third plurality of memory cells, the third plurality of memory cells storing information related to a corresponding portion of said first plurality of memory cells;

an extension decoder circuit for selecting ones of said third plurality of memory cells; and

an extension sensing circuit to detect content of said selected ones of said third plurality of memory cells.

42. The data storage system of claim 41 further comprising:

a second extension array including a fourth plurality of memory cells for storing information related to a corresponding portion of the second plurality of memory cells related to the content addressable memory; and

a second extension decoder for selecting a portion of the fourth plurality of memory cells,

wherein the extension sensing circuit detects content of selected portion of said fourth plurality of memory cells.

43. The data storage system of claim 40 wherein the configurable sense circuit comprises:

a sensing mode configuration circuit coupled to the selected ones of the first or second plurality of memory cells to detect content stored in said selected memory cells in said first or second sensing modes;

a first transistor of a first type including first and second terminals with a channel therebetween, and a gate for controlling current in said channel and coupled to the sensing mode configuration circuit, said first terminal being coupled to a supply voltage;

a current source including a first terminal coupled to the second terminal of the first transistor of the first type and a second terminal coupled to ground, the current source providing a bias current; and

a comparator for comparing the voltage on said second terminal of the first transistor of the first type and a reference voltage and including an output indicative of said comparison.

44. The data storage system of claim 43 wherein the sensing mode configuration circuit comprises:

a first transistor of a second type including first and second terminals with a channel therebetween, and a gate for controlling current in said channel, the second terminal being coupled to one of the selected ones of the first or second plurality of memory cells and coupled to the gate of the first transistor of the first type;

a first switch including a first terminal coupled to a supply voltage and including a second terminal coupled to the first terminal of the first transistor of the second type to selectively couple the supply voltage to said first transistor of the second type in said first sensing mode;

a second switch including a first terminal coupled to the first terminal of the first transistor of the second type, and including a second terminal coupled to the gate of the first transistor of the second type to selectively couple said first terminal of the first transistor of the second type to said gate in said first sensing mode;

a third switch including a first terminal coupled to said selected one of the memory cells and including a second terminal coupled to a ground terminal, to selectively ground said selected memory cell in said first sensing mode;

a fourth switch including a first terminal coupled to the first terminal of the first transistor of the second type and including a second terminal coupled to said ground terminal to selectively couple said first terminal to said ground terminal in said second sensing mode;

a fifth switch including a first terminal coupled to the gate of said first transistor of the second type and including a second terminal coupled to a bias voltage terminal to selectively couple said bias voltage terminal to said gate in said second sensing mode; and

a sixth switch including a first terminal coupled to the supply voltage, including a second terminal coupled to the selected memory cell to selectively couple said memory cell to said supply voltage in said second sensing mode.

45. A configurable sense amplifier comprising:

a comparator having first input coupled to gate reference voltage terminal, having a second input coupled to a detected voltage terminal and having an output for generating an output signal indicative of the comparison between voltages applied to the first and second terminals; and

a configurable detection circuit coupled to the detected voltage terminal to provide a voltage indicative of content in a selected memory cell, said voltage being done in a voltage sensing mode or in a current sensing mode.

46. The configurable sense amplifier of claim 45 wherein the sensing mode configuration circuit provides an adjustable bias to the voltage terminal that is dependent on sensing mode.

47. The configurable sense amplifier of claim 45 further comprising a second buffer/gain stage.

48. The configurable sense amplifier of claim 47 wherein the second buffer/gain stage includes an adjustable bias.

49. The configurable sense amplifier of claim 48 wherein the comparator includes an adjustable bias.

50. The configurable sense amplifier of claim 45 further comprising a second buffer/gain stage that is a source follower.

51. The configurable sense amplifier of claim 45 further comprising a comparator stage.

52. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells for storing content therein, a decoder circuit for selecting ones of said plurality of memory cells, and a sensing circuit to selectively detect content of said selected ones of said plurality of memory cells; and

a memory controller to perform a first memory operation on a first one of said memory arrays and perform a second memory operation on a second one of said memory arrays concurrently, said first and second ones of the memory arrays storing first and second type of content, respectively.

53. The data storage system of claim 52 wherein said first and second memory operations are selected from one of program, erase, and read.

54. The data storage system of claim 53 wherein said first and second types of content are selected from the group of code and data.

55. The data storage system of claim 52 wherein said first and second types of content are selected from the group of code and data.

56. The data storage system of claim 52 further comprising an extension array, wherein said memory controller performs said first memory function on a first one of said memory array and performs a third function on said extension memory array.

57. The data storage system of claim 52 further comprising a content addressable memory, and wherein said memory controller performs said first memory operation and performs a third memory operation on said content addressable memory concurrently.

58. The data storage system of claim 52 wherein the first memory operation is programming, the first one of said memory arrays stores data, the second memory operation is erasing and the second one of the memory arrays stores code.

59. The data storage system of claim 52 wherein the first memory operation is programming, the first one of said memory arrays stores data, the second memory operation is programming, and the second one of the memory arrays stores code.

60. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells for storing content therein, a decoder circuit for selecting ones of said plurality of said memory cells, and a sensing circuit to select the content of said selected ones of said plurality of memory cells; and

an interface controller to perform interface logic depending on the selected memory array or depending on an external interface.

61. The data storage system of claim 60 further including an IO driver controller.

62. The data storage system of claim 60 further including a general purpose memory controller.

63. The data storage system of claim 62 wherein the general purpose memory controller handling production and/or screen testing.

64. A data storage system comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells for storing content therein, a decoder circuit for selecting ones of said plurality of memory cells, and a sensing circuit to selectively detect content of said selected ones of said plurality of memory cells; and

an IO driver controller to perform an appropriate IO driver interface depending on the selected memory array or depending on external interface.

65. The data storage system of claim 64 further including an interface controller.

66. The data storage system of claim 64 further including a general purpose memory controller.

67. The data storage system of claim 66 wherein the general purpose memory controller handles production and/or screen testing.

68. A data storage system comprising:

a content addressable memory including a plurality of multilevel memory cells;

a decoder circuit for selecting ones of said second plurality of memory cells of said content addressable memory; and

a sensing circuit to detect content of said selected ones of said second plurality of memory cells.

69. The data storage system of claim 68 further comprising:

a tag bit memory for storing tag bit indicators of content stored in corresponding ones of the first plurality of memory cells.

70. The data storage system of claim 69 further comprising:

a tag bit sensing circuit to detect a selected tag bit indicator corresponding to selected ones of said first plurality of memory cells.

71. The data storage system of claim 68 further comprising:

a second memory array including a second plurality of memory cells;

a 2nd decoder circuit for selecting ones of said second plurality of memory cells;

72. The data storage system of claim 71 further comprising:

a second sensing circuit to selectively detect using a first or second sensing mode content of said selected ones of said second plurality of memory cells, the first and second sensing mode being determined by the selected tag bit corresponding to the selected memory cells;

73. The data storage system comprising:

an extension array comprising a 1st plurality of memory cells, the 1st plurality of memory cells being configurable to a number of memory levels;

an extension decoder circuit for selecting ones of said 1st plurality of memory cells; and

an extension sensing circuit to detect content of said selected ones of said 1st plurality of memory cells.

74. The data storage system of claim 73 wherein the sensing circuit configures the sensing mode according to the configurability of memory cells.

75. The data storage system of claim 73 further comprising:

a tag bit memory for storing tag bit indicators of content stored in corresponding ones of the first plurality of memory cells.

76. The data storage system of claim 75 further comprising:

a tag bit sensing circuit to detect a selected tag bit indicator corresponding to selected ones of said first plurality of memory cells.

77. The data storage system comprising:

an array comprising a first plurality of memory cells, the first plurality of memory cells being configurable to a number of memory levels and arranged in a plurality of array sectors, a security key stored for each array sector;

a decoder circuit for selecting ones of said first plurality of memory cells; and

a sensing circuit to detect content of said selected ones of said first plurality of memory cells.

78. The data storage system of claim 77 further including a sensing circuit to sense security key.

79. The data storage system comprising:

an array comprising a first plurality of memory cells, the first plurality of memory cells being configurable to a number of memory levels and arranged in a plurality of array sectors, a security measure stored for each array sector;

a decoder circuit for selecting ones of said first plurality of memory cells; and

a sensing circuit to detect content of said selected ones of said first plurality of memory cells.

80. The data storage system of claim 79 wherein the security measure comprising a disabling a security memory area.

81. The data storage system of claim 79 wherein the security measure comprising altering a security memory area.

82. A data storage system comprising:

a memory comprising a plurality of memory arrays, each memory array including a plurality of memory cells for storing content therein,

a first one of said memory arrays executing a first memory operation and a second one of said memory arrays executing a second memory operation concurrently,

said first and second memory arrays storing first and second type of content, respectively.

83. The data storage system of claim 82 wherein the memory is monolithic.

84. The data storage system of claim 82 wherein the first memory operation is programming, the first one of said memory arrays stores data, the second memory operation is erasing and the second one of the memory arrays stores code.

85. The data storage system of claim 82 wherein the first memory operation is programming, the first one of said memory arrays stores data, the second memory operation is programming, and the second one of the memory arrays stores code.